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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,515	12/27/2001	Dong Yeung Kwak	0465-0870P	9371

2292 7590 07/12/2004

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EXAMINER	
NGUYEN, HOAN C	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/026,515	KWAK ET AL.	
	Examiner	Art Unit	
	HOAN C. NGUYEN	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *4/23/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-15 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-15 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23 April 2004 has been entered.

Applicant cancelled claims 6-7, 16-19 and 21. Therefore, only claims 1-5, 8-15 and 20 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 1-5, 8-15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimada et al. (US00RE37591E).

In regard to claims 1 and 2, Shimada et al. teach (Figs. 2, 3, 4, 5B) a display panel including

- a first substrate having an array region and an array peripheral region as shown in Fig. 3.
- a second substrate having color filters 20a/b which overlaps to function as light shielding acting like black matrix (see below),
- the display panel comprising:
    - o a plurality of gate lines 2 on the first substrate;
    - o a gate insulating film on the first substrate including the gate lines; this is enhanced feature of active matrix LC display;
    - o a plurality of data lines 3 arranged to cross the gate lines, for defining a pixel region on the array region;
    - o a light leakage prevention (light shield 9) film formed between the gate lines of the array peripheral region (light shield 9 covers gate lines and region between gate lines), for preventing light leakage in areas where the color-mixing light-shielding 20a/b (acting like black matrix) is not formed, the array peripheral region (Fig. 3 col. 48-49) excluding pixel electrode as shown in Fig. 4 or 14.
    - o a TFT 1 and a pixel electrode 6 formed in each pixel region.
    - o a liquid crystal layer 25 formed between the first and second substrates.

wherein

- the light leakage prevention film is formed simultaneously with at least one of the gate lines (col. 6 lines 54-59) according to claim 4.

- the light leakage prevention film is formed to prevent an electrical short with the data lines due to gate insulating formed above gate lines and light shield 9 (claim 5).

In regard to claims 9-10, Shimada et al. teach (Figs. 2, 3, 4, 5B) a display panel including a method for manufacturing a display panel including a first substrate having an array region and an array peripheral region, and a second substrate having color filters which overlaps to function as light shielding acting like black matrix (see below), the method comprising the steps of:

- forming a plurality of gate lines 2 on the first substrate;
- forming a gate insulating film on the first substrate including the gate lines; this is enhanced step for forming active matrix LC display.
- forming a plurality of data lines 3 to cross the gate lines and define a pixel region on the array region;
- forming a light leakage prevention (light shield 9) film formed between the gate lines of the array peripheral region (light shield 9 covers gate lines and region between gate lines), for preventing light leakage in areas where the color-mixing light-shielding 20a/b (acting like black matrix) is not formed, the array peripheral region (Fig. 3 col. 48-49) excluding pixel electrode as shown in Fig. 4 or 14.
- forming a TFT 1 at a crossing point of a corresponding one of the gate lines and a corresponding one of the data lines;
- forming a passivation film 8 on the first substrate including the TFT; and

- forming a pixel electrode 6 coupled with the TFT on the passivation film.
- forming a liquid crystal layer between the first and second substrates.

wherein

- the light leakage prevention film is formed simultaneously with at least one of the gate lines to prevent light leakage in the display panel (col. 6 lines 54-59) according to claims 12.
- the light leakage prevention film is formed of a conductive material having a high reflectivity since the light-shielding pattern (light leakage prevention film) 9 is formed in the same patterning step as that of the gate lines 2 which are made of Aluminum (col. 5 lines 53-55 and col. 6 lines 57-58) according to claims 13-14.
- the light leakage prevention film is formed to prevent an electrical short with the data lines due to gate insulating formed above gate lines and light shield 9 (claim 15).

However, Shimada et al. fail to disclose a display panel comprising

- the second substrate having the black matrix and a color filter layer and facing the first substrate (claims 3 and 11);
- a capacitor metal layer to partially overlap an upper portion of one of the gate lines (claim 8 and 20).

Shimada et al. disclose (col. 2 lines 19-21) that it is conventional a display panel comprising a black matrix is generally provided on the color filters formed on the counter

substrate (second substrate) to prevent color mixing and light leakage. Shimada et al. disclose a second substrate having color filters which overlaps to function as light shielding, which can be replaced by a black matrix for preventing color mixing and light leakage (col. 2 lines 19-21). Furthermore, the overlapping of color filters to function as light shielding has ***an advantage*** of reducing production cost, but the overlapping of color filters has ***a disadvantage*** of generating the color mixing, which deteriorates color purity.

It is also well known art that a capacitor metal layer to partially overlap an upper portion of one of the gate lines (claim 8 and 20) for providing a constitution of storing capacities.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a display panel as Shimada et al. disclosed with (a) a black matrix is generally provided on the color filters formed on the counter substrate (second substrate) for preventing color mixing and light leakage; (b) a capacitor metal layer (capacitor electrode) to partially overlap an upper portion of one of the gate lines (claim 8 and 20) for providing a constitution of storing capacities.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (571)

272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim H Robert can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAN C. NGUYEN
Examiner
Art Unit 2871

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TARIFUR R. CHOWDHURY
PRIMARY EXAMINER